REMARKS

Applicant appreciates the Examiner's thorough review of the application and allowance of Claim 3, which has been rewritten in independent form.

Reconsideration and allowance of claims 1, 2, and 4 are requested.

Claims 1, 2, and 4 are patentable under 35 U.S.C. 103(a) over Jewett et al. (US No. 6,263,452) in view of Lanus et al. (US No. 6,112,271).

The subject matter of claims 1, 2, and 4 is not obvious from the references.

Claims 1, 2, and 4 are not obvious and are patentable over Jewett et al. (US No. 6,263,452) in view of Lanus et al. (US No. 6,112,271). Neither reference teaches or suggests all of the limitations of any of the claims. Claim 1 points out that "if one of the CPU boards is down, the system is restored by detaching said down CPU board from said bus and attaching said detached CPU board to said bus again." Claim 4 points out that the "control system is restored by detaching the said down CPU board from said bus and attaching said detached CPU board to said bus again." Claim 2 depends from claim 1 and shares this limitation. No reference teaches or suggests this simple way of restoring a system, which is an important feature of the present invention.

Jewett teaches a computer system with multiple, identical CPUs and memory modules. Jewett's CPUs are loosely synchronized and execute the same instruction stream and its memory modules store duplicates of the same data. The system detects faults in the CPUs and memory modules and places a faulty unit offline for replacement while continuing operation. (See Abstract) However, Jewett requires numerous complicated steps to restore its system after a fault, such as determining status, selective shut off of the I/O processors, issuing a reset command to the shut off

processor, etc. (See Col. 27, lines 5 - 48). Jewett does not teach "if one of the CPU boards is down, the system is restored by detaching said down CPU board from said bus and attaching said detached CPU board to said bus again." Additionally, Jewett does not teach a control system comprising a bus arbiter and a non-volatile memory and having periodically executed functions and passive functions or a system controller to continue processes only by periodically executed functions and passive functions of a hardware structure of the system such that when one of the CPU boards on the bus is down while accessing the non-volatile memory, the system controller assigns the right to use the bus to another CPU board.

Lanus discloses a mutliconfiguration backplane that can be configured four different ways. The four different configurations are dual, extended, active/standby, and active/active. The mutliconfiguration backplane has two compact PCI buses each with a system processor slot, a bridge slot, and a set of one or more input/output slots. Additionally, there is a cross connection between the first system processor slot and the second bridge slot and a second cross connection between the second system processor slot and the first bridge slot.

Lanus fails to teach a management module having only periodically executed functions and passive functions. Also, Lanus is silent on a system controller comprising a bus arbiter and non-volatile memory.

Lanus teaches that increasing the number of slots available on a certain bus is desirable. However, providing a different backplane for each configuration is inefficient for the manufacturer and seller. Accordingly, Lanus discloses a backplane that is capable of multiple configurations.

Lanus fails to teach or suggest a control system comprising a bus arbiter and a non-volatile memory and having periodically executed functions and passive functions or a system controller to continue processes only by periodically executed functions and passive functions of a hardware structure of the system such that when one of the CPU boards on the bus is down while accessing the non-volatile memory, the system controller assigns the right to use the bus to another CPU board.

For at least this reasons, the rejection of Claims 1 and 4 under 35 U.S.C. 103(a) is improper and should be withdrawn. Claim 2 depends on Claim 1 and therefore should be allowed as well.

Claim 2 adds the patentable feature that "if one of the CPU boards or power sources is down, the system is restored by detaching said down CPU board or said down power source from said bus and attaching said detached CPU board or said detached power source to said bus again as power for the whole system is supplied." For the same reasons as discussed above, no reference teaches or suggests this feature. Lanus does not disclose "duplex power" in Col. 3, lines 8-35. Furthermore, the term "duplex power" or the like are not found in Lanus. Claim 2 specifies unique features that are not taught by any cited reference. For at least these reasons, the rejections of Claims 2 under 35 U.S.C. 103(a) is improper and should be withdrawn.

For at least the above reasons the rejection of Claims 1, 2, and 4 is improper and should be withdrawn.

CONCLUSION

Reconsideration and allowance are respectfully requested.

Respectfully,

James C. Wray, Reg. No. 22,693
Clifford D. Hyra, Reg. No. 60,086
1493 Chain Bridge Road, Suite 300
McLean, Virginia 22101
Tel: (703) 442-4800
Fax: (703) 448-7397

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